

REMARKS

Claims 45 and 51 have been canceled. Claims 1-44, 46-50 and 52 -57 are still pending in this application. It is acknowledged that claims 37 and 49 have been allowed.

Reconsideration of the application is earnestly requested.

Objection to the Specification

The specification has been objected to because claim 39 recites a "machine readable medium" and the specification does not provide proper antecedent basis. Accordingly, claim 39 has been amended to require a "computer readable medium" and it is now believed that this objection should be withdrawn. The Examiner has indicated that the specification does disclose a "computer readable medium."

Double Patenting Rejection

The Office action has rejected claims 1, 13, 25 and 39 under the judicially-created doctrine of obviousness-type double patenting in view of claims 1, 13, 24 and 34 of U.S. Patent No. 7,107,567. To obviate the provisional double patenting rejection, Applicant has previously submitted a terminal disclaimer pursuant to 37 C.F.R. §1.321. Applicant therefore respectfully requests that the double patenting rejection be withdrawn.

Claim Rejections under 35 USC §101

Claim 25 and 39 have been rejected because the inventions are directed to non-statutory subject matter. Claims 25 and 39 now recite "a tangible computer readable medium" and is submitted that these claims are directed to statutory subject matter.

Claim 39 has also been rejected because the claim is drawn to software per se and does not provide a practical application. It is submitted that claim 39 does provide a practical application because the computer program product includes both a programming version of the IP core and a simulation model of the IP core. The programming version allows an electronic design to function, whereas the simulation model specifically includes obfuscation circuitry designed to prevent a hardware implementation of the IP core.

It is therefore requested that these rejections under §101 be withdrawn.

Claim Rejections under 35 USC §112

Claims 1, 13, 25 and 39 have been rejected in that a step of "identifying" has been omitted. Claims 1, 13 and 25 have been amended to include a step of "identifying a region" within the electronic design to which obfuscation circuitry may be added. Claim 39 has not been amended because claim 39 is directed toward a computer program product that already includes a simulation model with obfuscation circuitry. The obfuscation circuitry is already present within the simulation model; there is no need to "identify a region" because there is no step of "adding obfuscation circuitry" in this claim 39.

Claims 1, 13, 25 and 39 have also been rejected in that they omit essential structural cooperative relationships of elements under MPEP §2172.01 (paragraph 13 at page 11 of the Office action). Applicant understands that the omitted relationships are "adding" and "creating," or perhaps the relationship between "adding" and "creating." In any case, Applicant submits that no structural relationships have been omitted. Applicant does not understand what possible structural cooperative relationship the Examiner is referring to. It is not necessary that there be a structural relationship between the steps of "adding" and "creating." The step of "creating" does create a simulation model using the obfuscated version of the electronic design, the obfuscated version having been created in the step of "adding" when obfuscation circuitry is added to the electronic design. In that sense, there is some relationship between the step of "creating" and the previous step of "adding." Therefore, a cooperative relationship is present. Furthermore, the Examiner questions how the creation of a simulation model is done. The "creating" step requires creating a simulation model using the electronic design. In general, the process of creating a simulation model is shown in Figure 2. The paragraph beginning at line 23 at page 15 also describes creating a simulation model using model writer 214. Because a model writer is known in the art, it is submitted it is not necessary to explain in elaborate detail how the model writer functions. Therefore, it is requested that this rejection of claims 1, 13, 25 and 39 be withdrawn.

Claims 40-45 have been rejected as being indefinite because of the term "substantially." This term has been removed from these claims.

Claims 8 and 20 have been amended to require the term "or" instead of the term "and/or." Therefore, it is submitted that these claims are no longer indefinite because the alternative term "or" is acceptable claim language and indicates that the claim should be interpreted to encompass either of the alternatives.

Applicant respectfully submits that the above amendments to the claims address the Examiner's rejections under §112.

Claim 1 Rejection under 35 USC §103

The Office action has rejected claim 1 under §103 as being obvious in view of *Jakubowski et al. (Jakubowski)* and *Meyer*. Although the Examiner's arguments have been carefully considered, Applicant respectfully traverses this rejection as explained below.

Claim 1 requires an "electronic design suitable for direct compilation into a practical hardware implementation of the electronic design." The Office action at page 5 indicates that the electronic design could be a design for a hardware module or a software module, and that *Jakubowski* teaches a design for a software module. But, the specification makes clear that an "electronic design" generally refers to the logical structure of an electronic device such as an integrated circuit (page 9, line 33-page 10, line 9) that is implemented in hardware. "Electronic design" does not refer to a design for a software module, and thus any software module disclosed by *Jakubowski* cannot anticipate this element.

Further, the Office action at top of page 6 states that the obfuscator 134 "could be implemented in a hardware module such as an integrated circuit." Perhaps, but the Examiner is confusing the digital goods 122 with the obfuscator 134. It is irrelevant that block 134 might be implemented in a hardware module; the digital goods 122 are only software and it is these digital goods that are being likened to the electronic design of claim 1.

Claim 1 requires, though, that the electronic design be suitable for direct compilation into a practical hardware implementation. The digital goods 122 are not suitable for direct compilation into a practical hardware implementation because they are not an electronic design. There is no disclosure in reference describing that digital goods 122 are suitable for direct compilation into a practical hardware implementation.

The Office action at page 6, paragraph c, argues that the digital goods 122 disclose the electronic design. But, this portion of reference only discloses that the digital goods are software or data; there is no disclosure of an electronic design that is suitable for direct compilation into a practical hardware implementation

The Office action at page 6, paragraph d, argues that it is well known that an unprotected electronic design can be compiled into a hardware implementation. The cited reference does not disclose this feature and the Examiner has not provided any evidence or declaration alleging that this fact is known.

The second step of claim 1 requires:

adding obfuscation circuitry to said electronic design to produce an obfuscated version of the electronic design.

The Office action cites column 5. But, this portion of the disclosure simply discloses "that randomly applied to various forms of protection to the segmented digital good." But, there is no disclosure in *Jakubowski* of any type of circuitry that is added to an electronic design. The various types of protection disclosed in *Jakubowski* only manipulate the software in some manner; no additional circuitry is being added. This step of claim 1 requires obfuscation circuitry that is added. The disclosure of "various forms of protection" does not in any way describe circuitry.

The second step of claim 1 also requires:

wherein said obfuscation circuitry prevents practical implementation of the electronic design on a target hardware device.

Again, column 5 of *Jakubowski* does not disclose any added circuitry that prevents implementation on a hardware device. The obfuscation techniques of *Jakubowski* might prevent illegal copying, or render illegal copies easily identifiable, but none of the techniques of *Jakubowski* prevent implementation of an electronic design on a hardware device. This portion of claim 1 requires circuitry that prevents implementation of the electronic design on a hardware device. *Jakubowski* does not disclose any of these features.

The third step of claim 1 requires:

creating a simulation model using said obfuscated version of said electronic design.

The Office action at page 7, paragraph f, states that "one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references." To the contrary, Applicant submits it is entirely appropriate to explain why one individual reference, in this case *Meyer*, does not teach a particular step of claim 1. If *Meyer* does not teach

this third step of claim 1, then there is no *prima facie* case of obviousness and the §103 rejection cannot stand.

The Office action cites both *In re Keller* and *In re Merck & Co.* But these are both following cases and do not have any reasoning or support in them for the cited language. These cases cite *In re Young and Humbert*, which in turn is also a following case without reasoning or support. *In re Young and Humbert*, in turn, cites *In re Goepfrich* and *In re Mapelsden*. *In re Mapelsden* also does not include the cited language. The only point made in *In re Mapelsden* is that "the issue lies in what the combination of references make obvious to the person of ordinary skill and not whether a feature of one reference can be bodily incorporated in the other to produce the subject matter claimed." In the present situation, Applicant is not attempting to argue that a feature of one reference cannot be bodily incorporated into the other reference.

What Applicant has argued is that none of the cited references disclose this third step of claim 1. Applicant argues that none of the cited references disclose "creating a simulation model using said obfuscated version of said electronic design." The Office action at page 18 does not allege that either reference discloses this step. The Office action at page 8, however, does allege that *Meyer* does teach this step in paragraph 72. Paragraph 72 states that "the model compiler vendor is able to shroud and/or obfuscate the object code without increasing simulator development difficulty." The Office action then states that "the obfuscation is already added by a compiler vendor before any simulation is done by the simulation vendor."

Applicant does agree that paragraph 72 indicates that the model compiler vendor (*i.e.*, the model compiler itself) is able to obfuscate the object code. Paragraphs 66 and 67 indicate that the model compiler accepts HDL source code and produces HDL object code in the form of linkable object files. It is clear that the obfuscation is performed by the model compiler after it inputs the HDL source code. But, claim 1 requires "creating a simulation model using said obfuscated version of said electronic design." Thus, the claim requires that the source electronic design is obfuscated before it is used to create a simulation model. By contrast, paragraph 72 of *Meyer* indicates that it is the model compiler itself that obfuscates the object code; the original HDL source code (without any obfuscation added to it) is input to the model compiler.

Further, there is no disclosure in *Meyer* that obfuscation circuitry is added to the electronic design. *Meyer* simply mentions the word "obfuscate" in paragraph 72 without any explanation as to what it means. In order for an anticipatory reference to be considered as prior

art, it must be enabling. Without any further explanation of the term "obfuscate," one of skill in the art would not understand that obfuscation circuitry should be added to an electronic design.

It is submitted that none of these above limitations of claim 1 are present in the references as cited, and it is requested that this rejection of claim 1 be withdrawn.

Claims 2-12 are dependent upon claim 1 and are submitted as being patentable for at least the reasons given above with respect to claim 1.

Rejection of Claims 13 and 25

The Office action has also rejected claims 13 and 25 under §103 as being obvious in view of *Jakubowski* and *Meyer*. Claims 13 and 25 each require similar limitations as claim 1 and are believed patentable for the same reasons given above. Claims 14-24 and 26-36 are dependent upon claims 13 and 25 respectively, and are submitted as being patentable for at least the reasons given above.

Rejection of claim 38

The Office action has also rejected claim 38 under §102 as being anticipated in view of *Koushanfar*. In the first place, claim 38 requires similar limitations as claim 1 and is believed patentable for the same reasons given above.

Further, claim 38 requires:

(c) inserting obfuscation circuitry into the region.

Koushanfar does not teach or suggest this step. Simply because the word "obfuscation" is used does not mean that the reference teaches inserting obfuscation circuitry. In order for a reference to be anticipatory prior art it must be enabling. One of skill in the art would not understand that "obfuscation" means "inserting obfuscation circuitry." It is suggested that the Office review the cited reference (reference [7]) to determine if this reference actually discloses "inserting obfuscation circuitry."

Claim 38 also requires:

(f) producing a simulation model using said optimized IP core that includes said inserted obfuscation circuitry.

There is no disclosure in *Koushanfar* of producing a simulation model. The Office action cites the Conclusion on page 4 but even here there is no discussion of producing a simulation model that includes the inserted obfuscation circuitry. While *Koushanfar* does mention in the first part of page 3 that an additional finite state machine may be added to design, there is no indication that this finite state machine is actually obfuscation circuitry that prevents the simulation model from being compiled into a practical hardware implementation. For these reasons, it is requested that the rejection of claim 38 be withdrawn.

Rejection of claim 39

The limitations of claims 45 and 51 have been incorporated into claim 39. It is submitted that none of the references disclose added obfuscation circuitry that increases the area of the core or reduces the speed of the critical path. Further, none of the references disclose a simulation model that not only contains obfuscation circuitry but is also cycle accurate and bit accurate.

Dependent Claims 46-50

Since the dependent claims depend from the independent claims, it is respectfully submitted that they are each patentable over the art of record for at least the same reasons as set forth above with respect to the independent claims. Further, each of the dependent claims require additional features that when considered in light of the claimed combination further distinguish the claimed invention from the art of record. For example, claims 46-50 each specifically require that the simulation model is cycle accurate and bit accurate. The advantage is that even though the simulation model might include some form of obfuscation circuitry that prevents a practical hardware implementation, the simulation model will still produce an accurate simulation result for a hardware developer. Claims 46-50 require a cycle accurate and bit accurate simulation model, terminology that is understood and appreciated by those of skill in the art.

Dependent Claims 40-44 and 52-57

Dependent claims 40-44 require that the added circuitry increase the area of the design. Dependent claims 40-44 and 52-57 are believed patentable for least the reasons set forth above with respect to their independent claims.

Reconsideration of this application and issuance of a Notice of Allowance at an early date are respectfully requested. If the Examiner believes a telephone conference would in any way expedite prosecution, please do not hesitate to telephone the undersigned at (612) 252-3330.

Respectfully submitted,
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